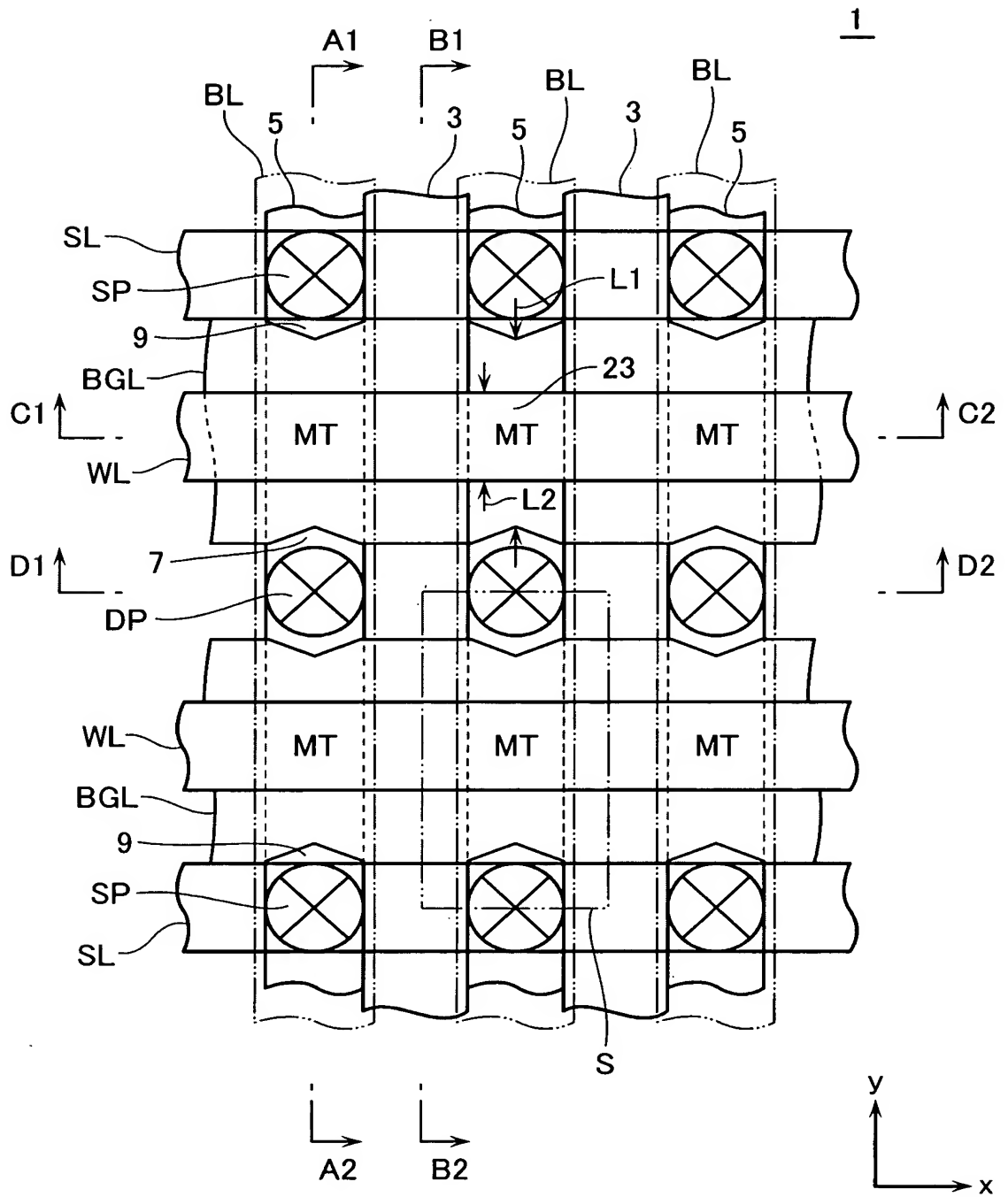


FIG. 1



[illegible]

[illegible]

This diagram shows a cross-sectional view of a semiconductor device. It features a grid of pillars (41) on a substrate (11). The pillars are separated by trenches (43). The device includes a base layer (11), a layer (13), and a layer (15) which together form a region 17. A layer (7) is also present. The pillars (41) are connected to a layer (3) and a layer (33). The pillars are labeled with 'BL' at the top. The device is divided into regions D1 and D2. A bracket labeled 'DP' groups the regions 51, 47, and 43. Other labels include 49, 45, 39, 3, and 11.

FIG. 3

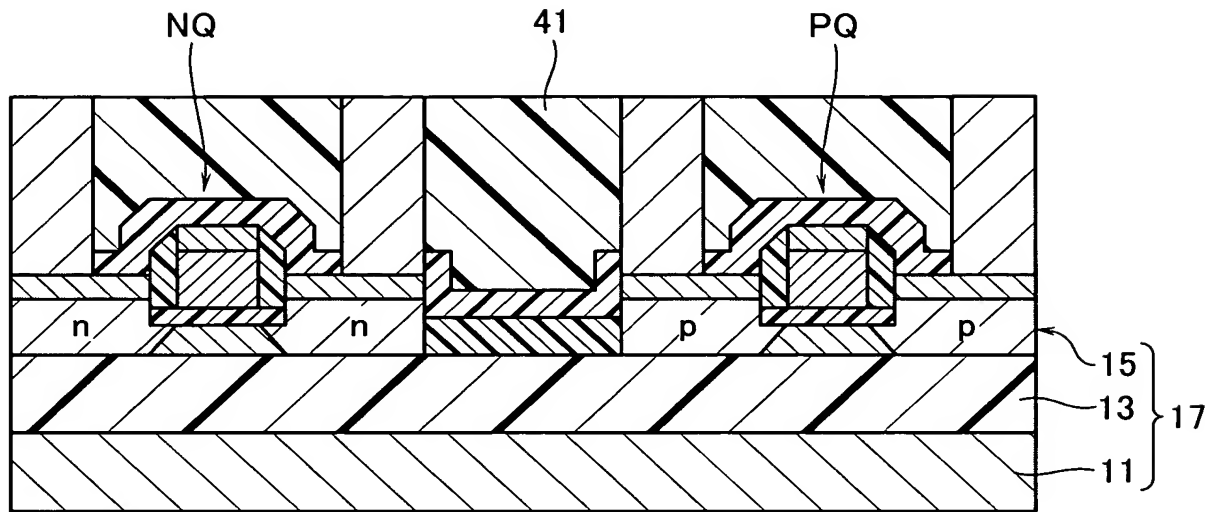


FIG. 4

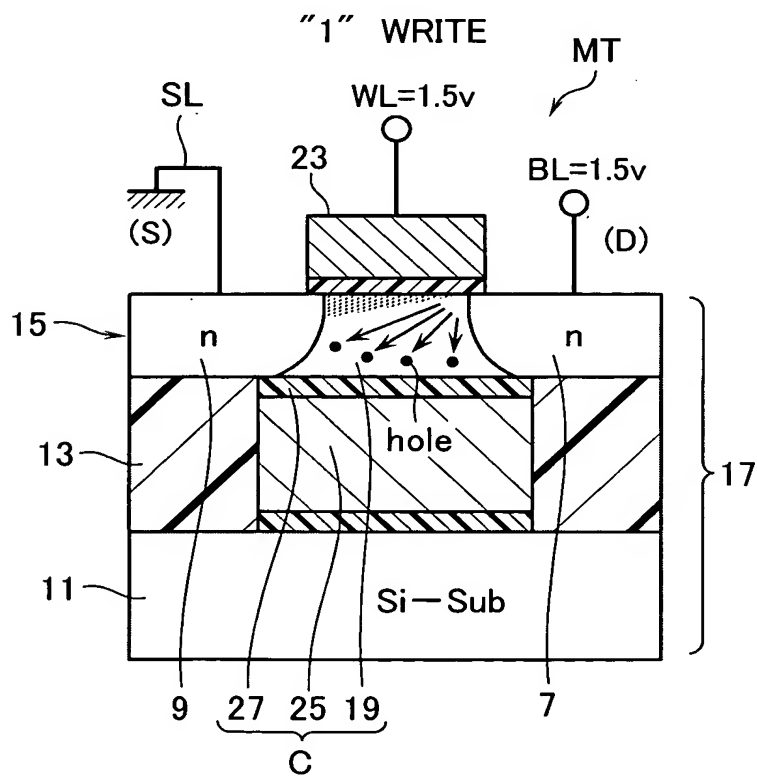


FIG. 5

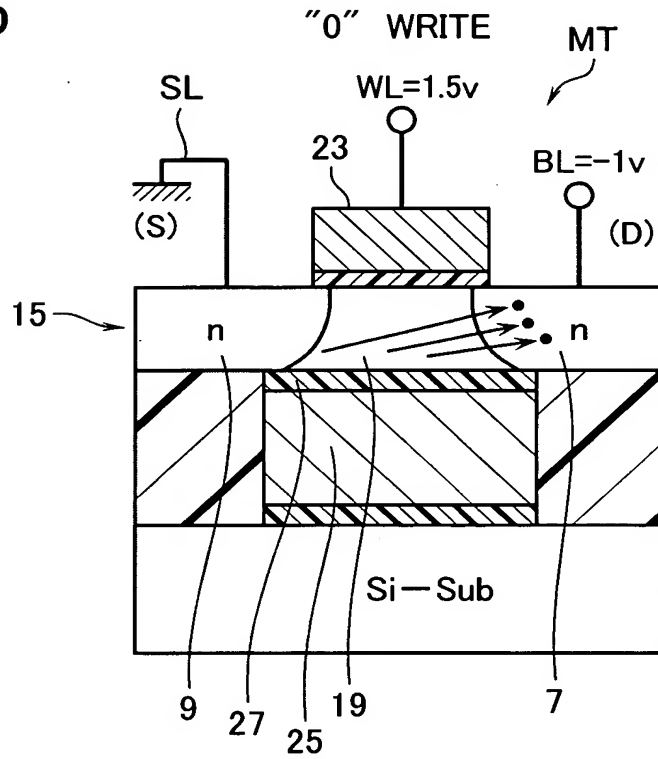
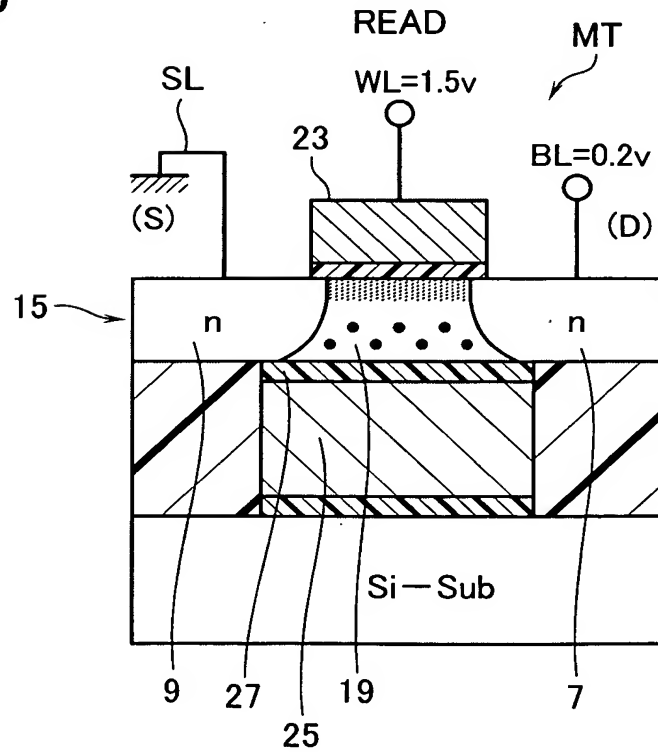


FIG. 6



Wiring layer

61

41

39

3

13

11

n-

n+

59

57

FIG. 9

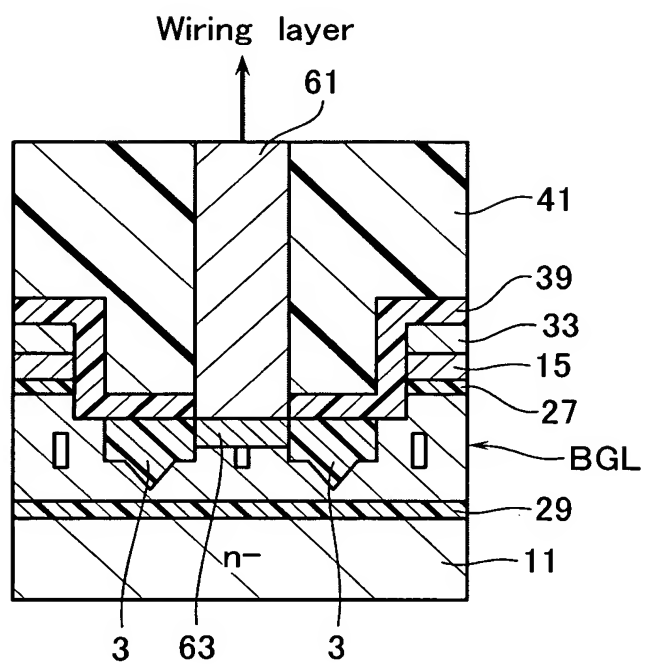


FIG. 10

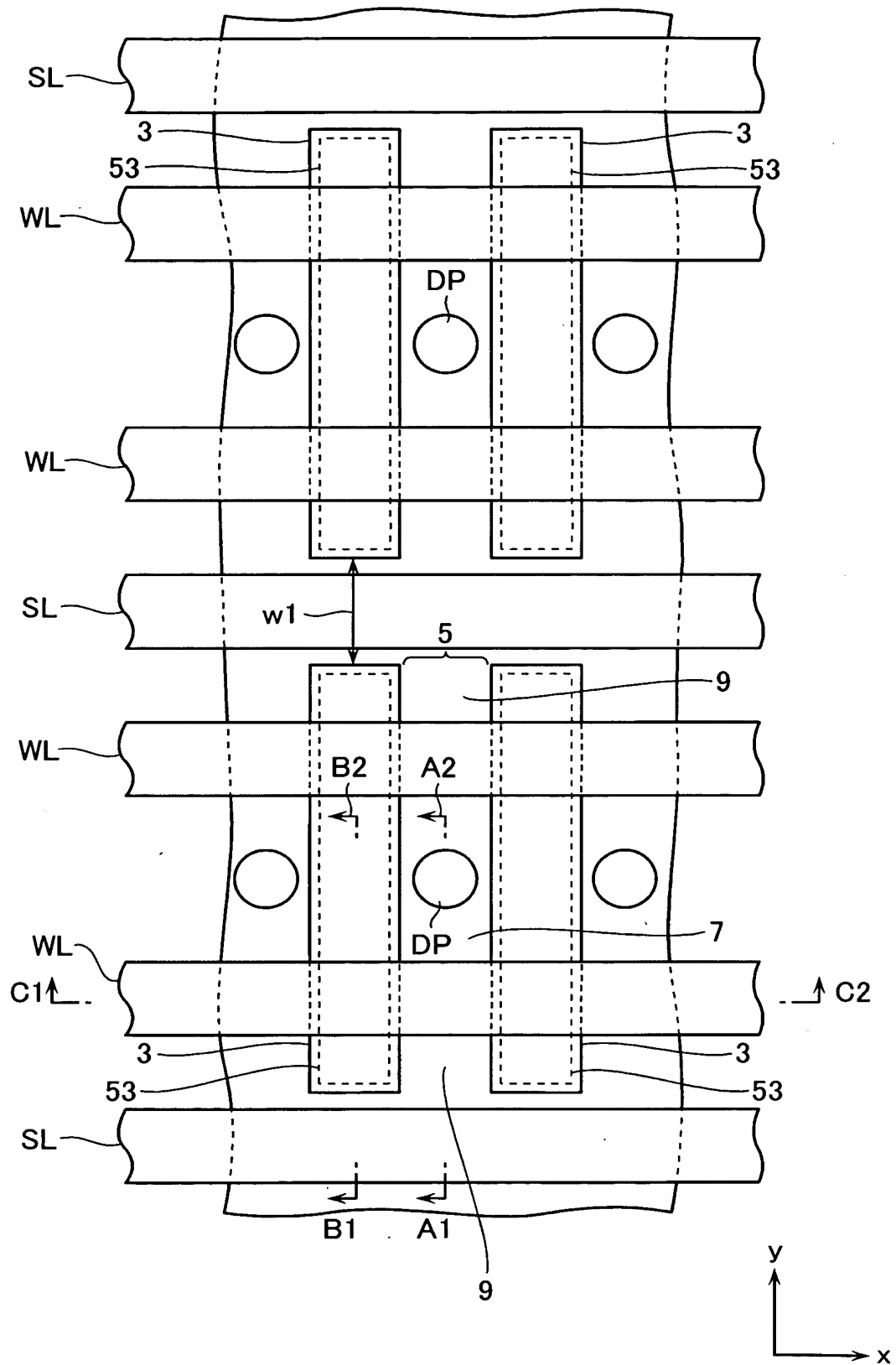




FIG. 11

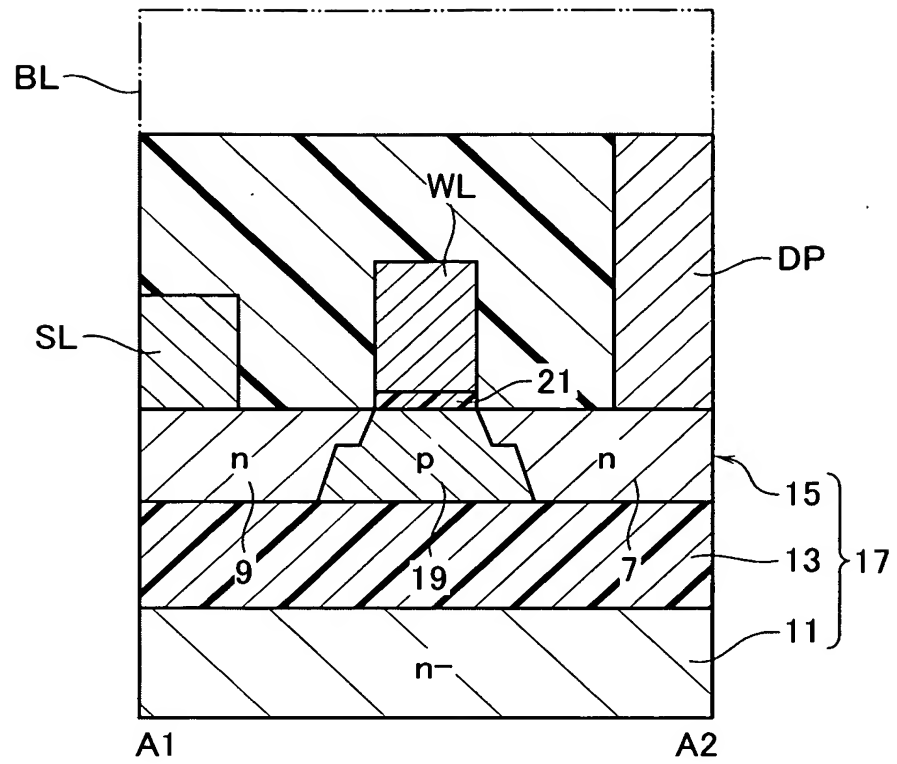


FIG. 12

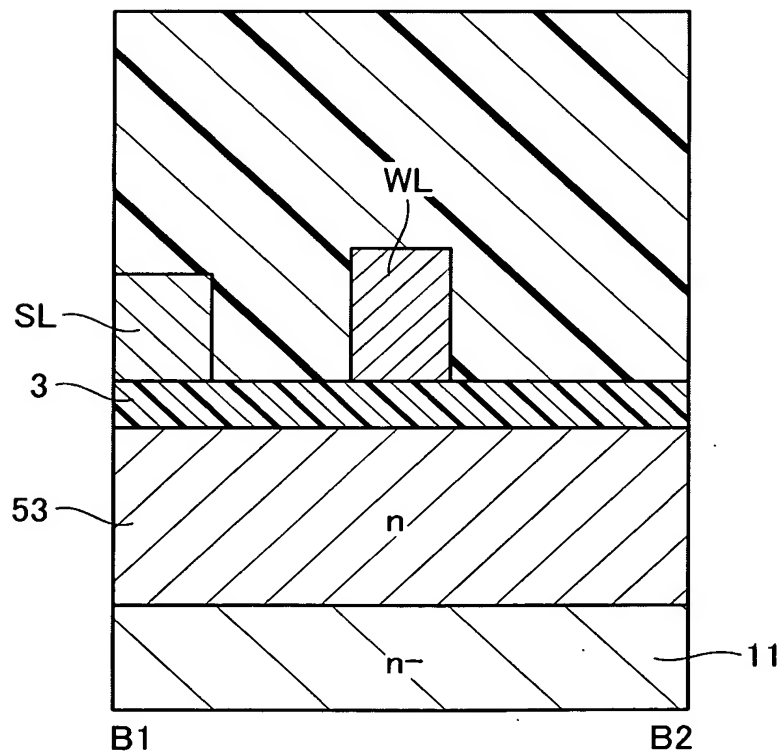


FIG. 13

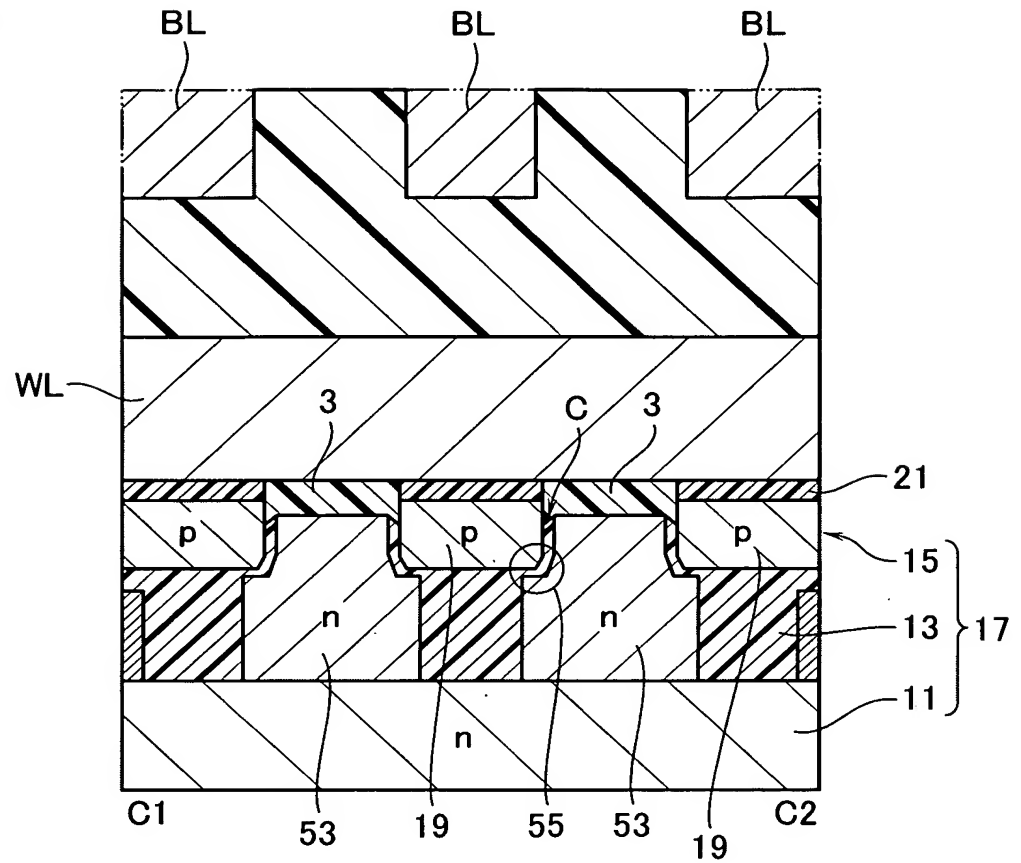


FIG. 14

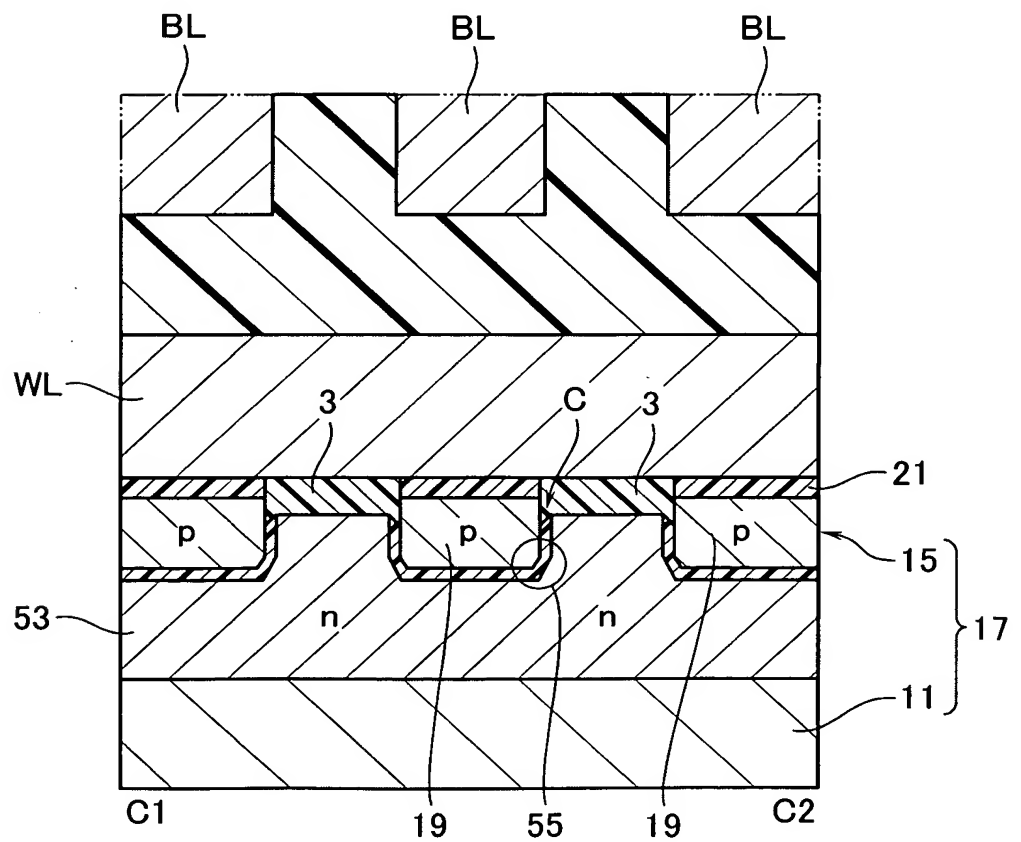


FIG. 15A

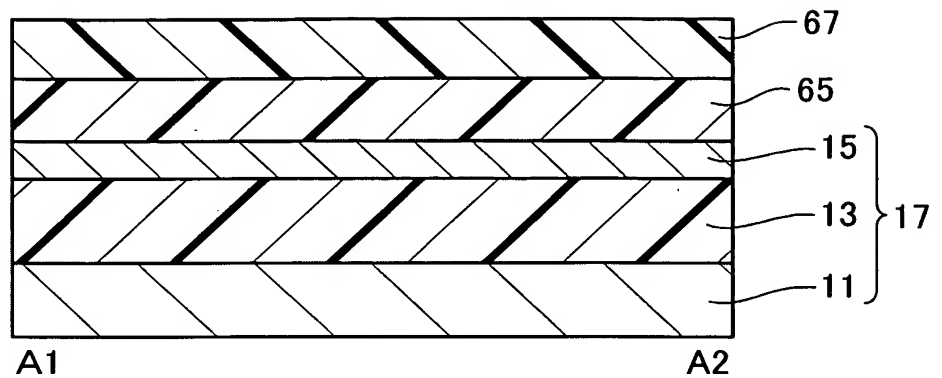


FIG. 15B

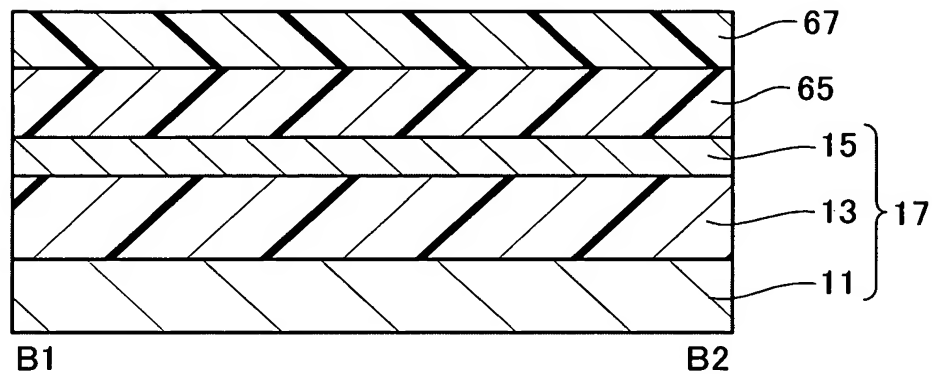


FIG. 15C

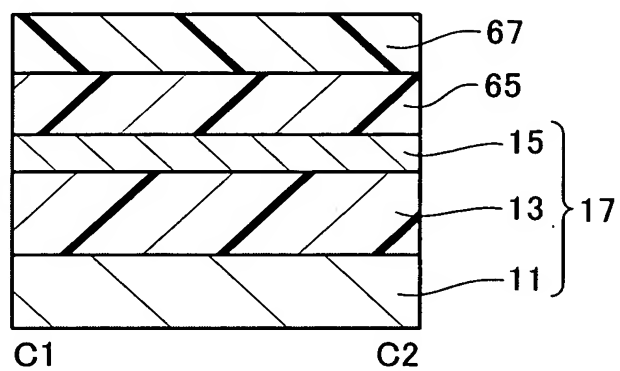


FIG. 15D

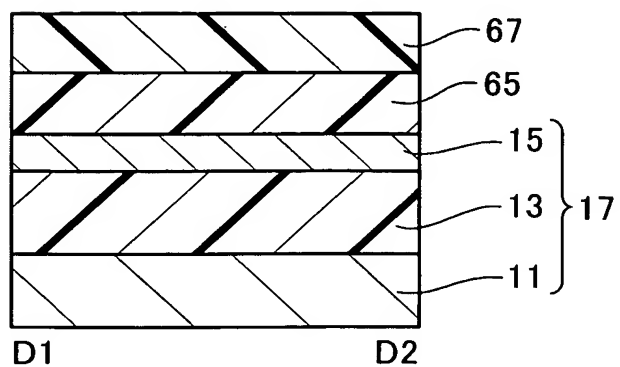


FIG. 16A

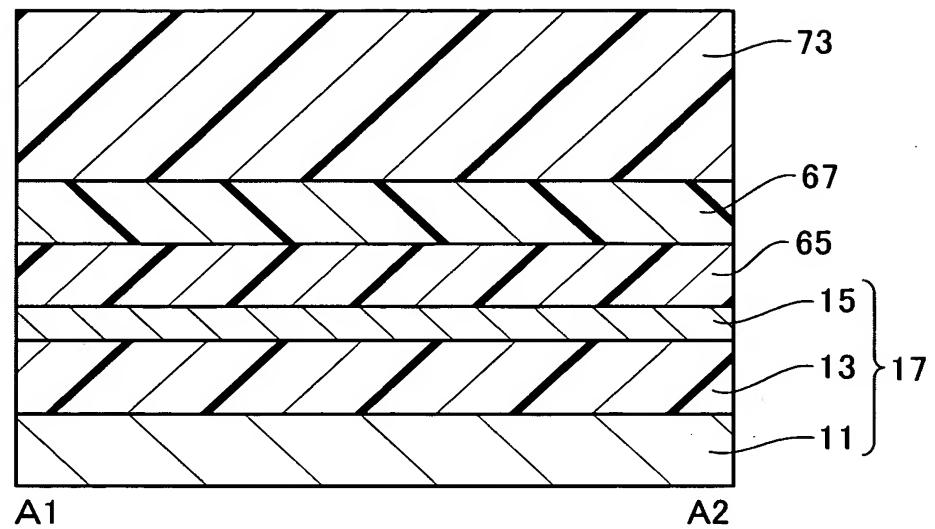


FIG. 16B

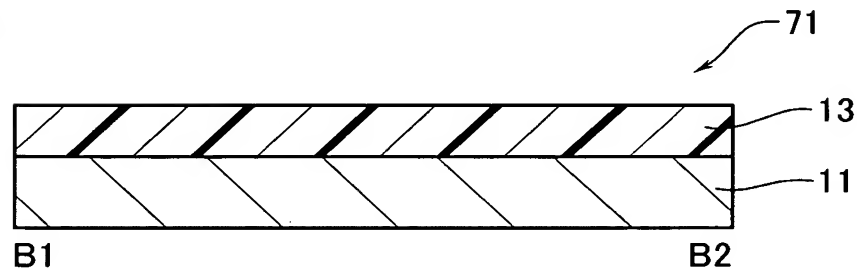


Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 11 with a base layer 13 and a patterned layer 15. A central channel 71 is formed by a mask 69, with side walls 67 and 65. The device is labeled C1 and C2 at the bottom.

A cross-sectional view of a semiconductor device. It features a U-shaped structure with three vertical pillars. The left and right pillars are filled with a material having diagonal hatching. The central pillar is empty. The base of the structure is a horizontal layer. Labels include: 69 (bracketed over the top of the pillars), 71 (pointing to the top of the central pillar), 73 (pointing to the top of the right pillar), 67 (pointing to the top surface of the right pillar), 65 (pointing to the side surface of the right pillar), 15 (pointing to the top surface of the base), 13 (pointing to the side surface of the base), 11 (pointing to the bottom surface of the base), 17 (bracketed over the base layer), D1 (pointing to the left side of the base), and D2 (pointing to the right side of the base).

FIG. 17A

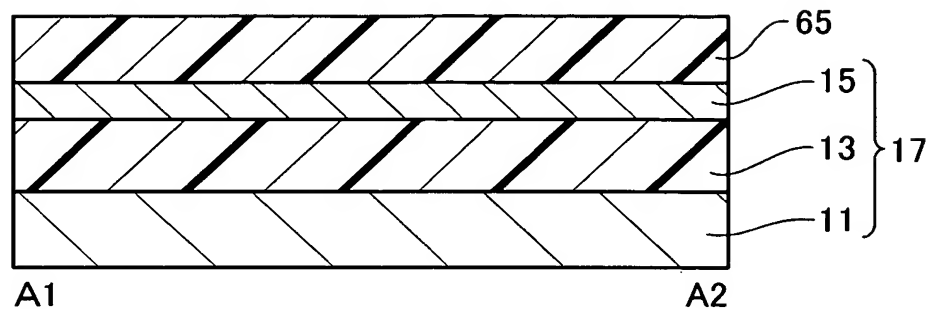


FIG. 17B

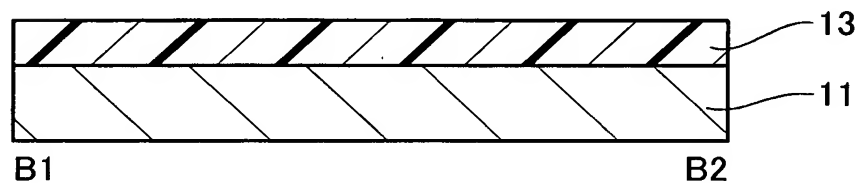


FIG. 17C

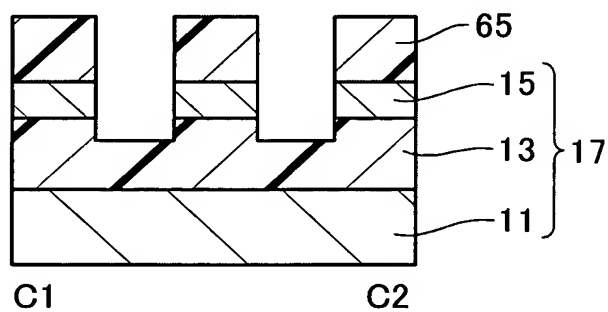


FIG. 17D

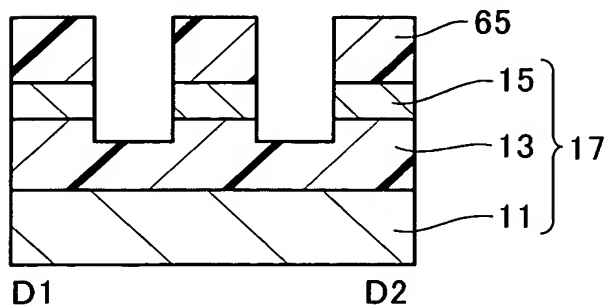


FIG. 18A

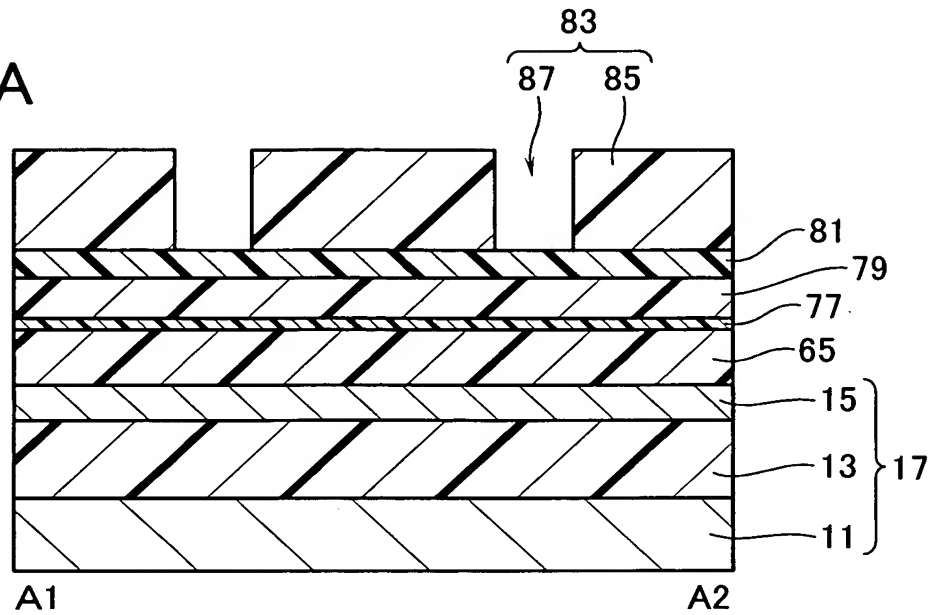


FIG. 18B

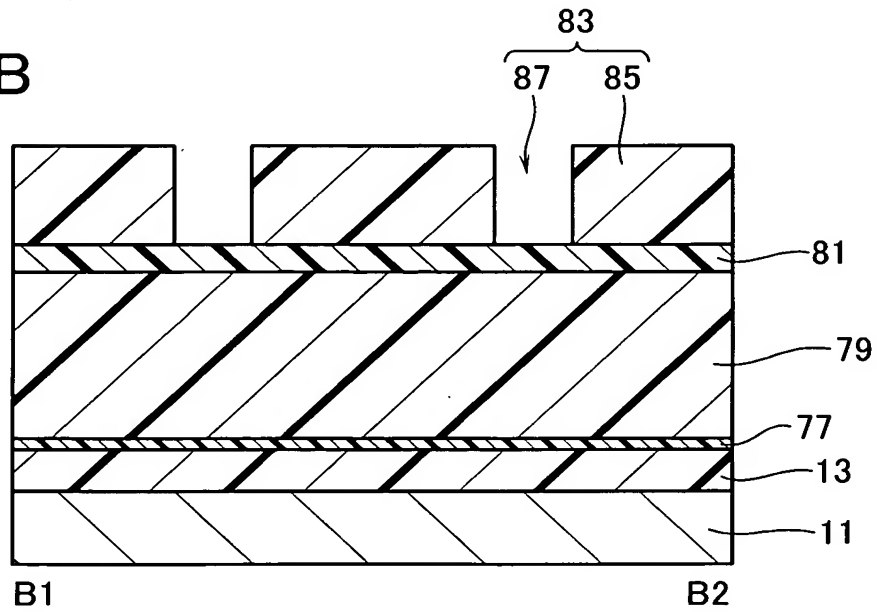


FIG. 18C

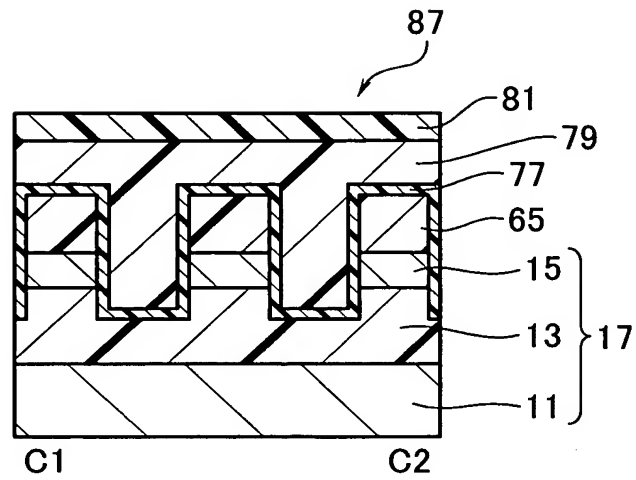


FIG. 18D

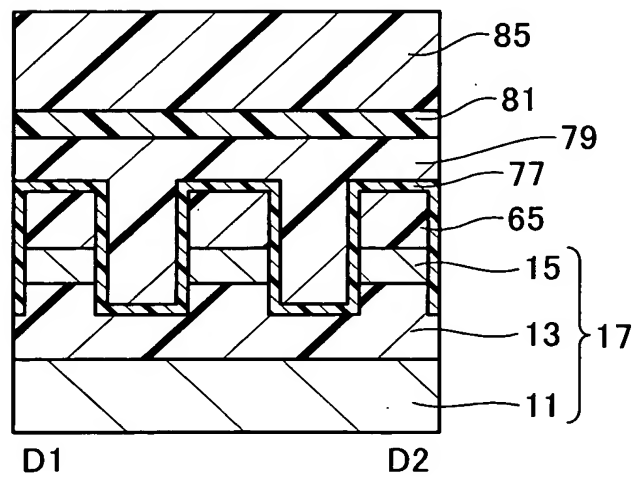




FIG. 19A

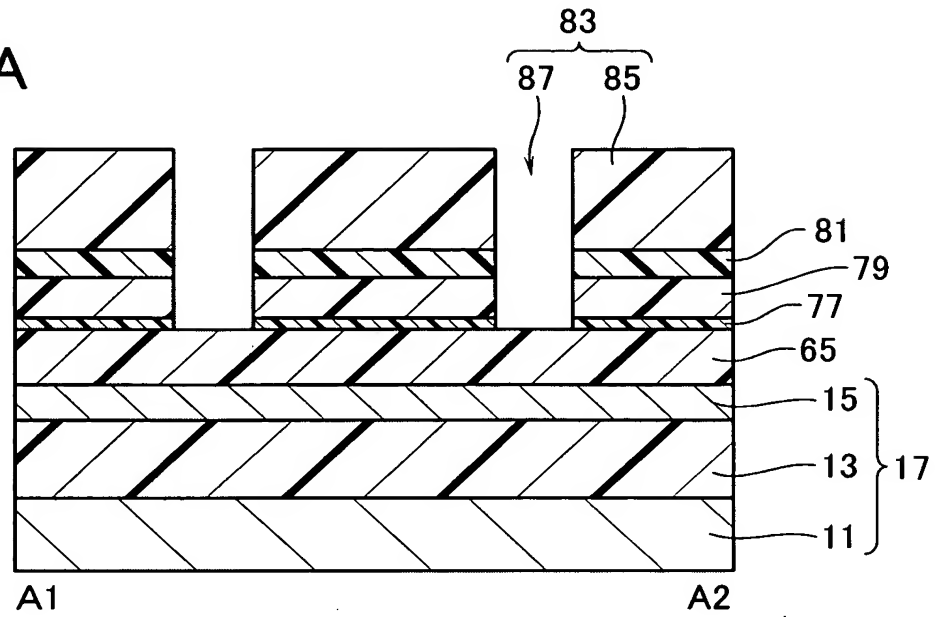


FIG. 19B

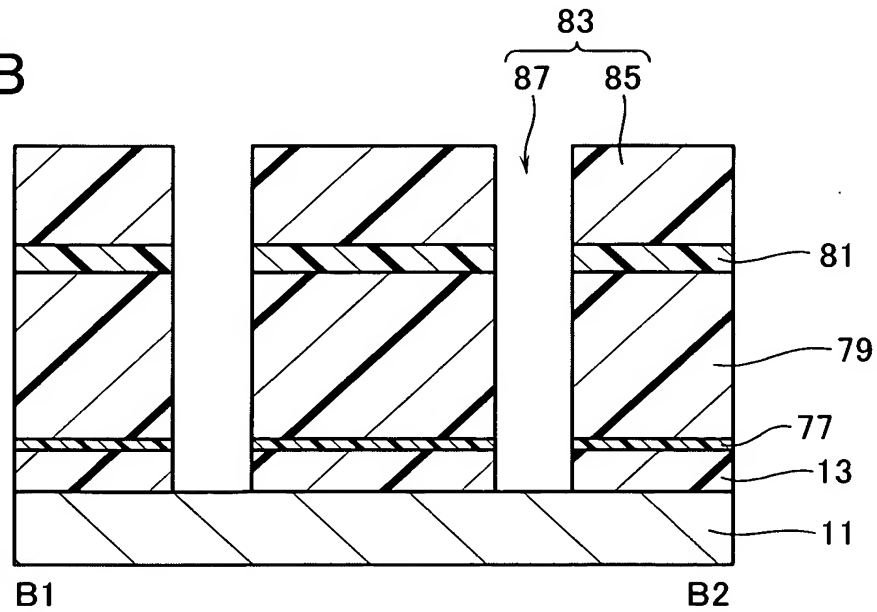


FIG. 19C

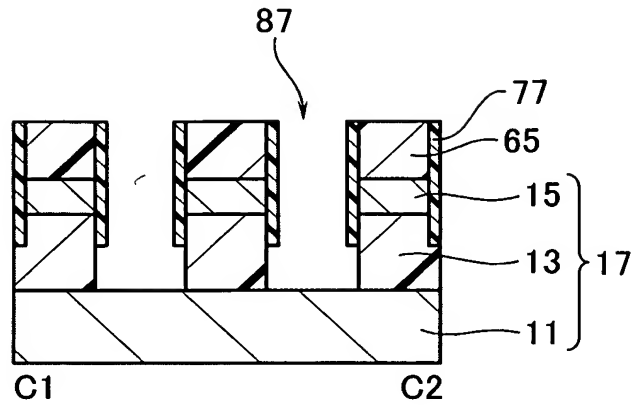


FIG. 19D

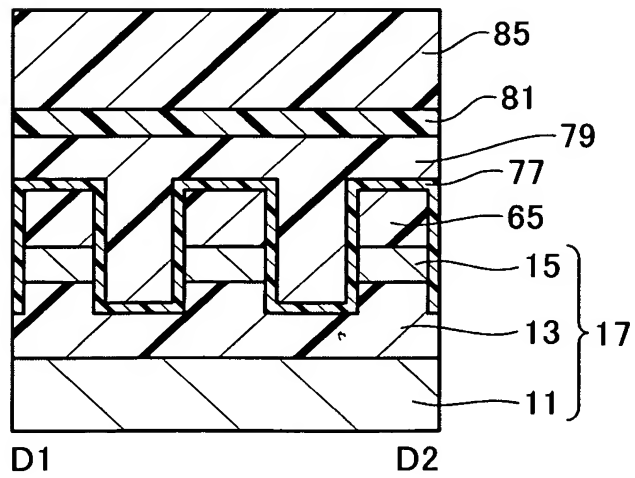


FIG. 20A

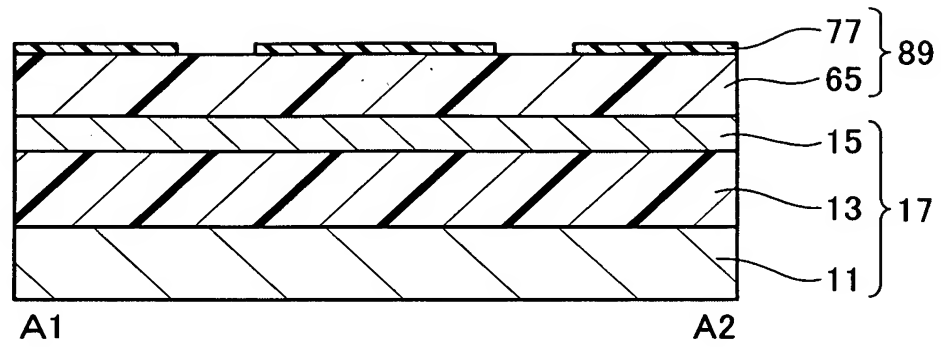


FIG. 20B

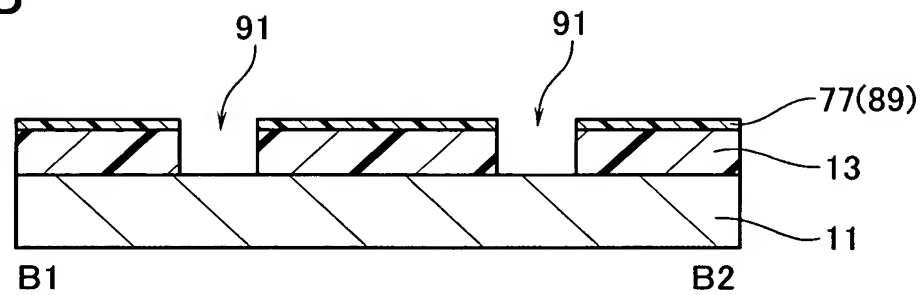


FIG. 20C

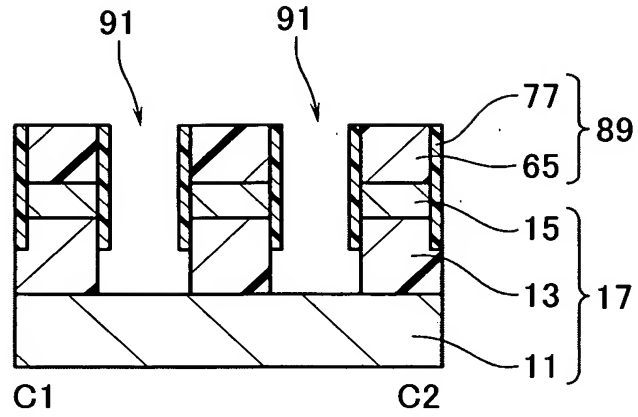


FIG. 20D

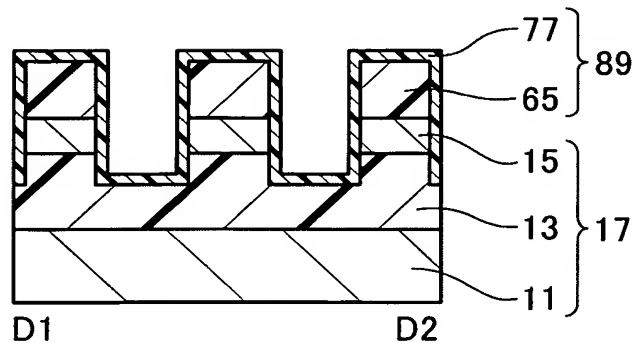


FIG. 21A

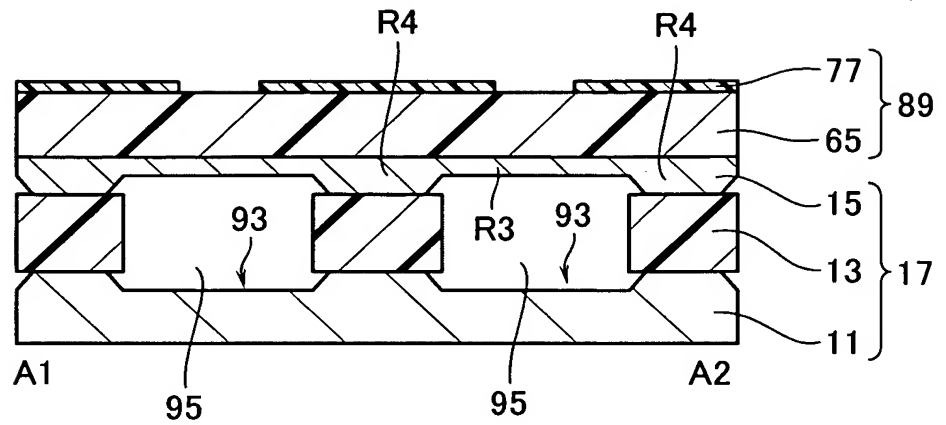


FIG. 21B

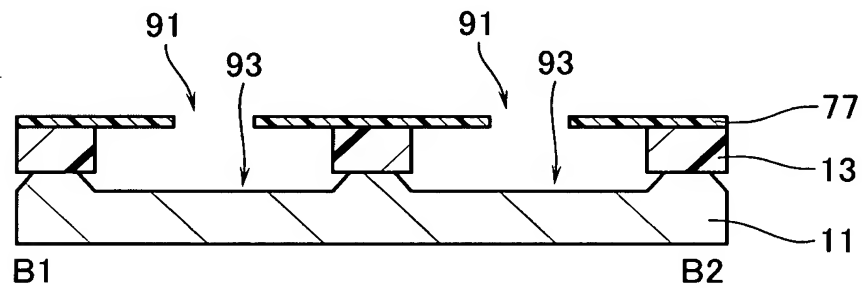


FIG. 21C

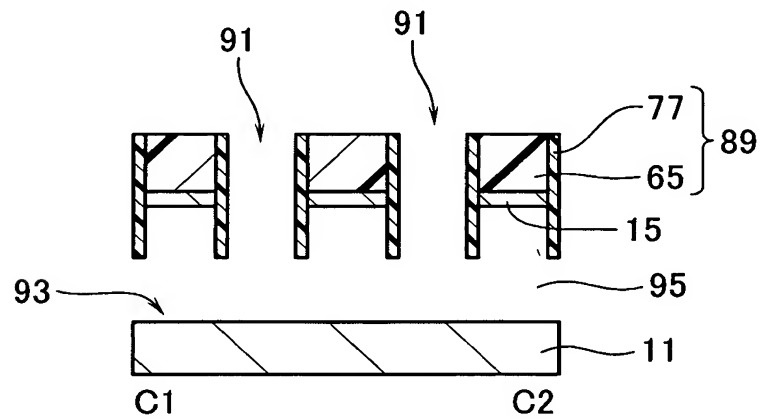


FIG. 21D

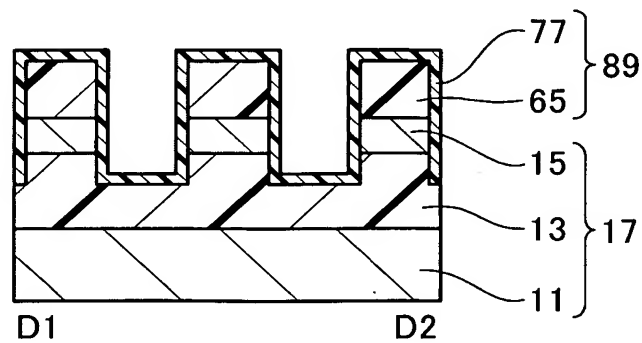


FIG. 22A

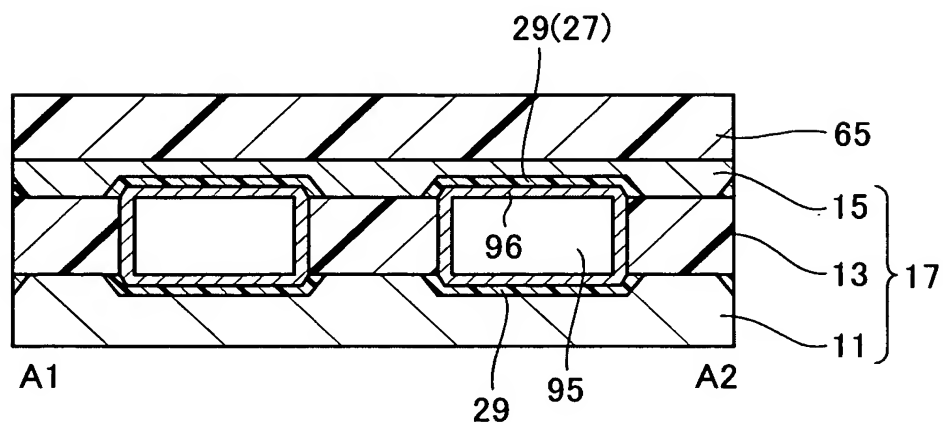


FIG. 22B

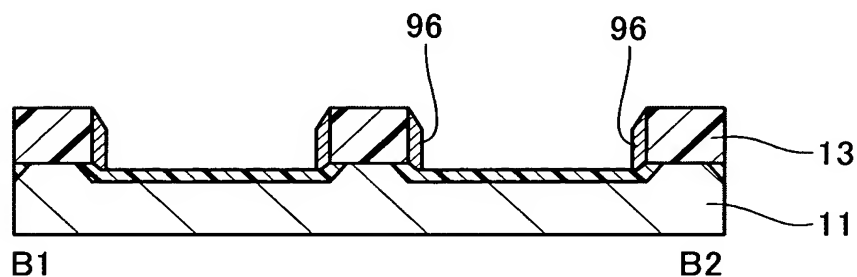


FIG. 22C

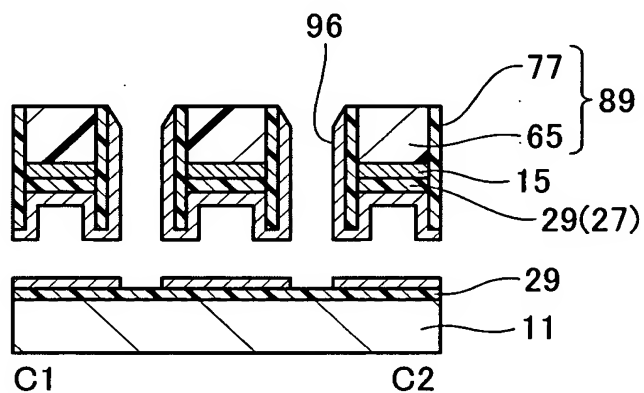


FIG. 22D

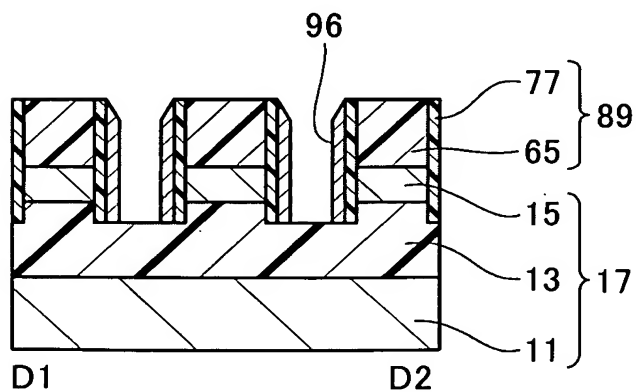


FIG. 23A

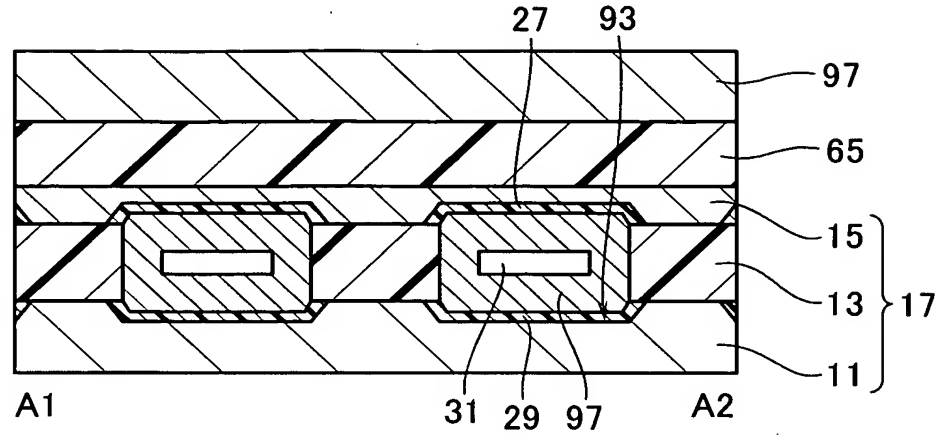


FIG. 23B

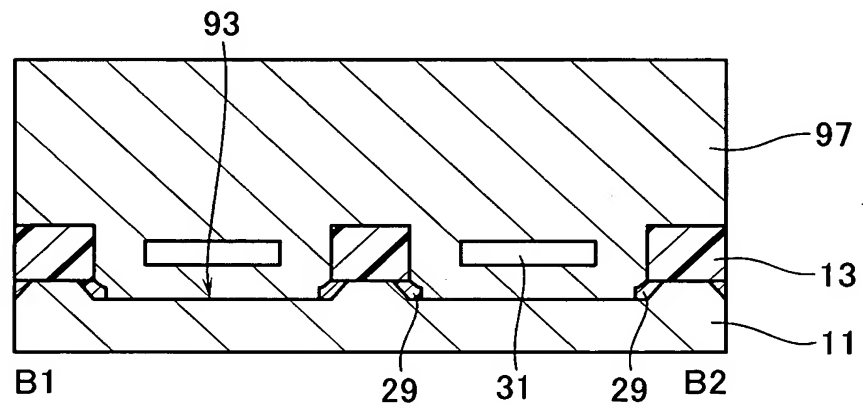


FIG. 23C

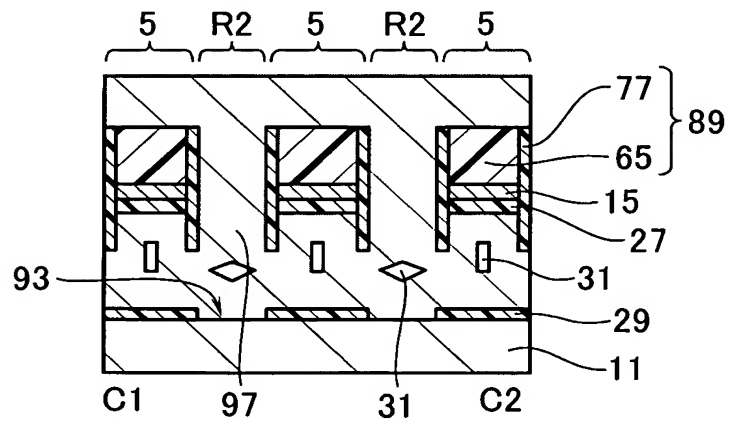


FIG. 23D

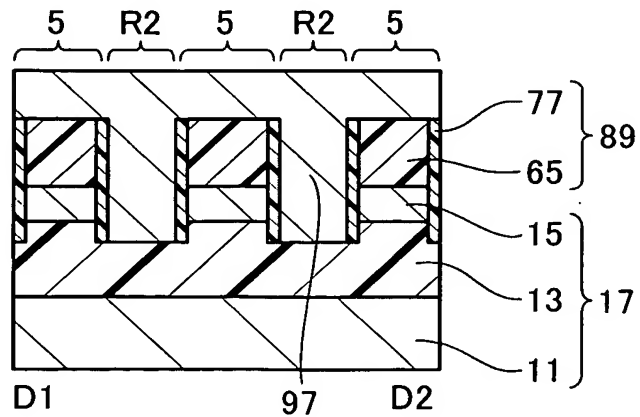


FIG. 24A

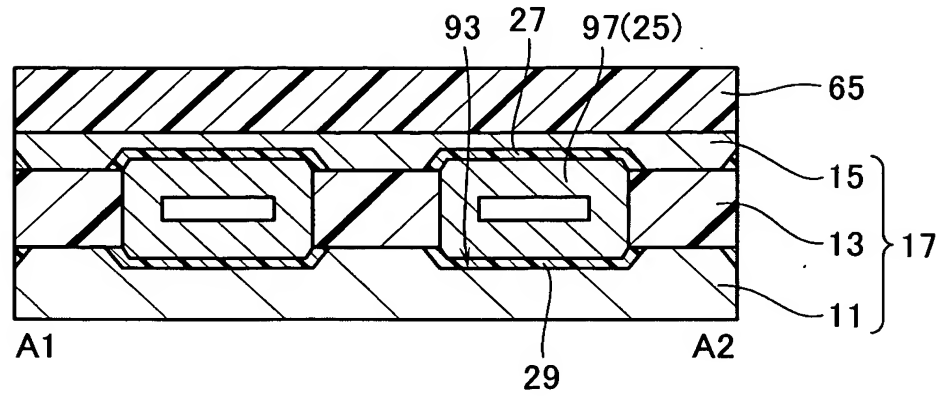


FIG. 24B

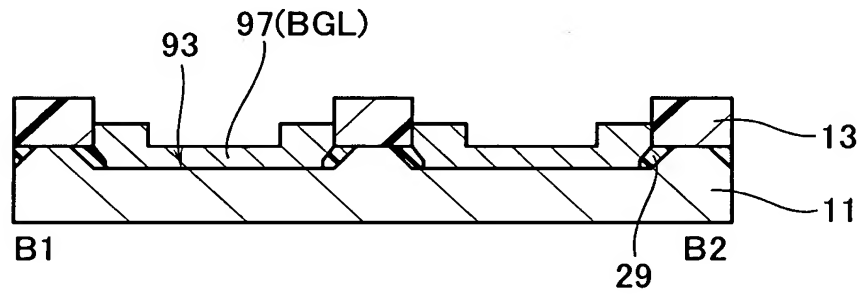


FIG. 24C

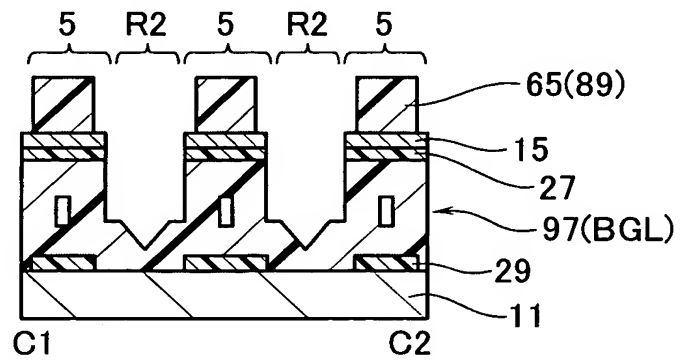


FIG. 24D

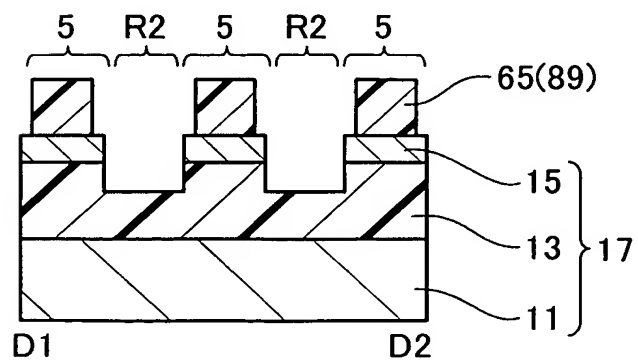




Diagram illustrating a cross-sectional view of a semiconductor device. The device includes a substrate 11, a conductive layer 29, and two semiconductor elements 15 and 13. A protective layer 65 is formed on top of the conductive layer 29. The device is shown in a cross-section along line A1-A2. Other labels include 93, 27, 25, 99, 15, 13, 11, A1, and A2.

Diagram illustrating a cross-sectional view of a semiconductor device. The device includes a substrate 11, a gate layer 13, and a gate electrode 93. A barrier layer (BGL) is formed on the gate electrode 93. The device is shown between contacts B1 and B2.

Diagram illustrating a cross-sectional view of a semiconductor device. The device structure includes a substrate 11, a base layer 27, and a gate layer 99. The base layer 27 is divided into regions 15 and 29. The gate layer 99 is divided into regions 65 and 27. The device is shown between contacts C1 and C2.

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 11, a layer 13, and a series of rectangular blocks 15. A layer 65 is formed on top of each block 15, and a layer 99 is formed on top of layer 65. The device is labeled D1 and D2 at the bottom.

FIG. 26A

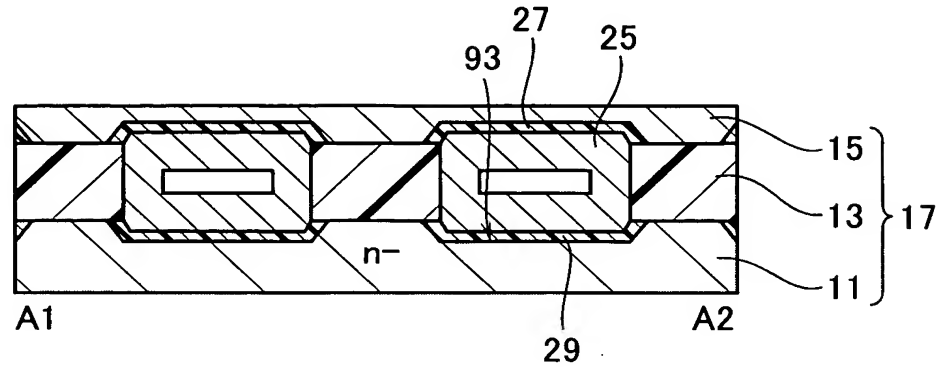


FIG. 26B

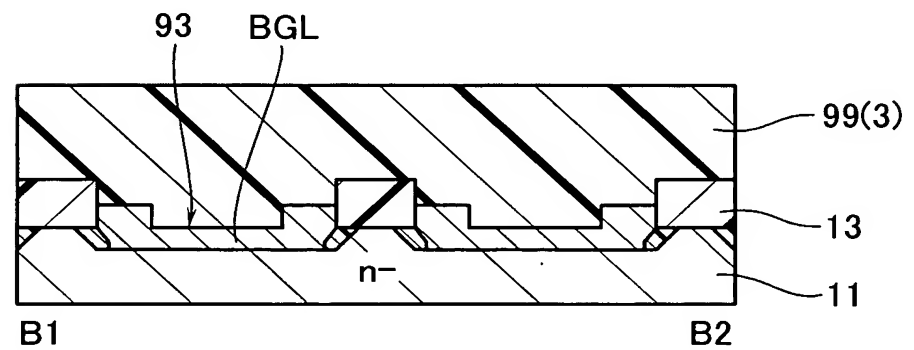


FIG. 26C

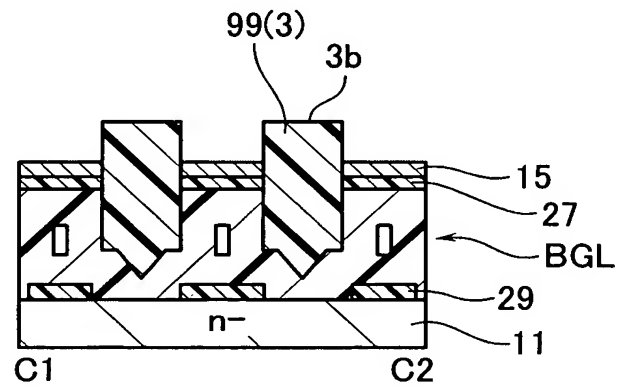


FIG. 26D

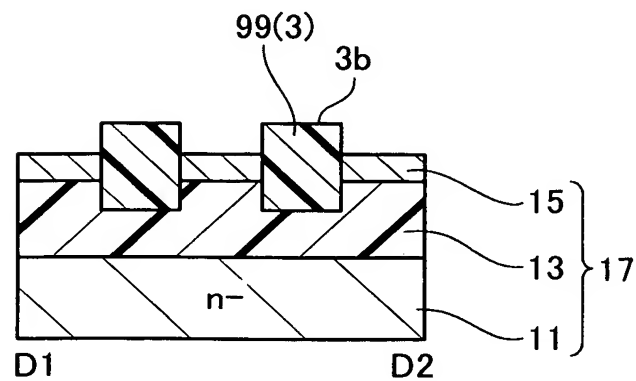


FIG. 27

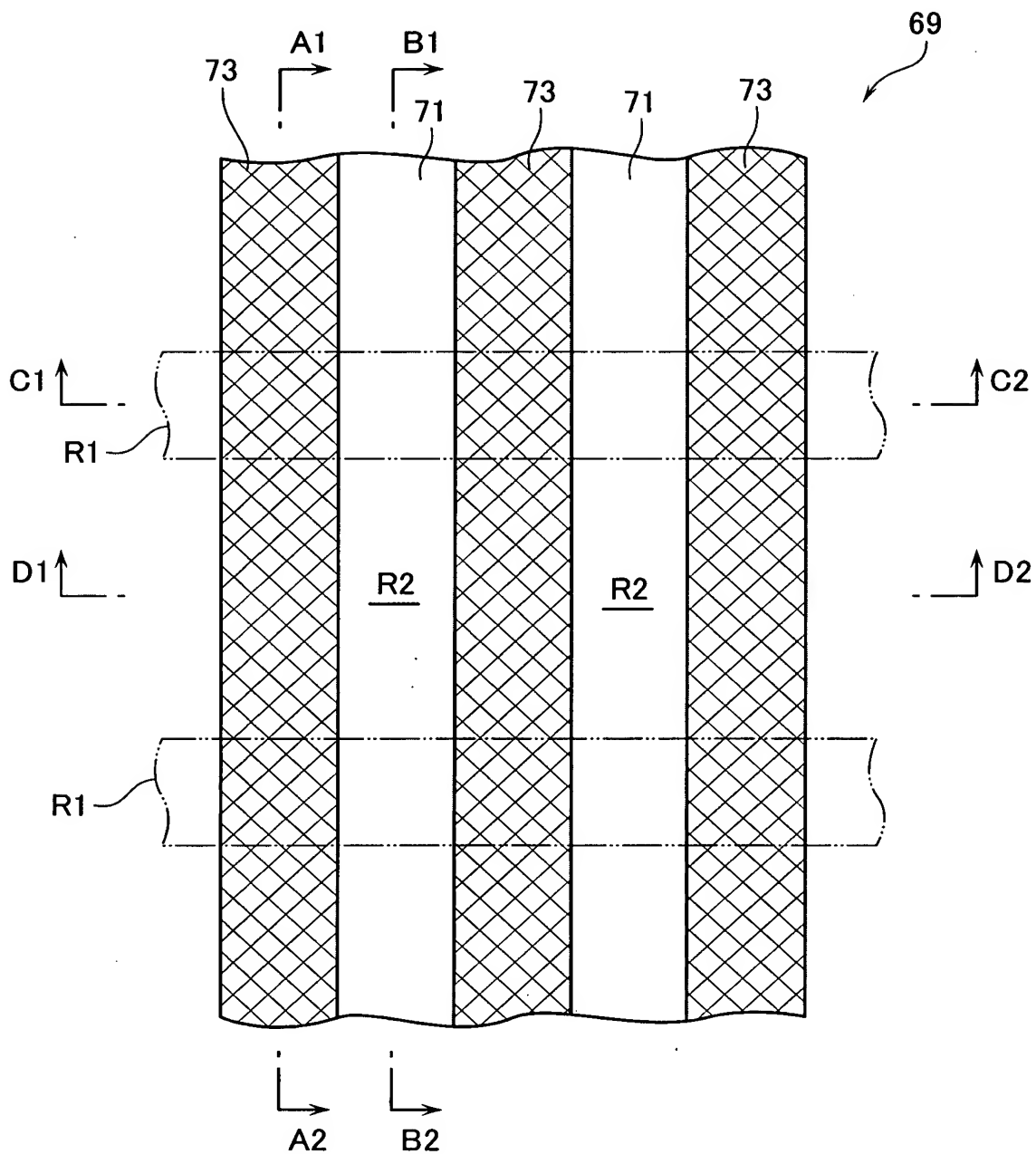


FIG. 28

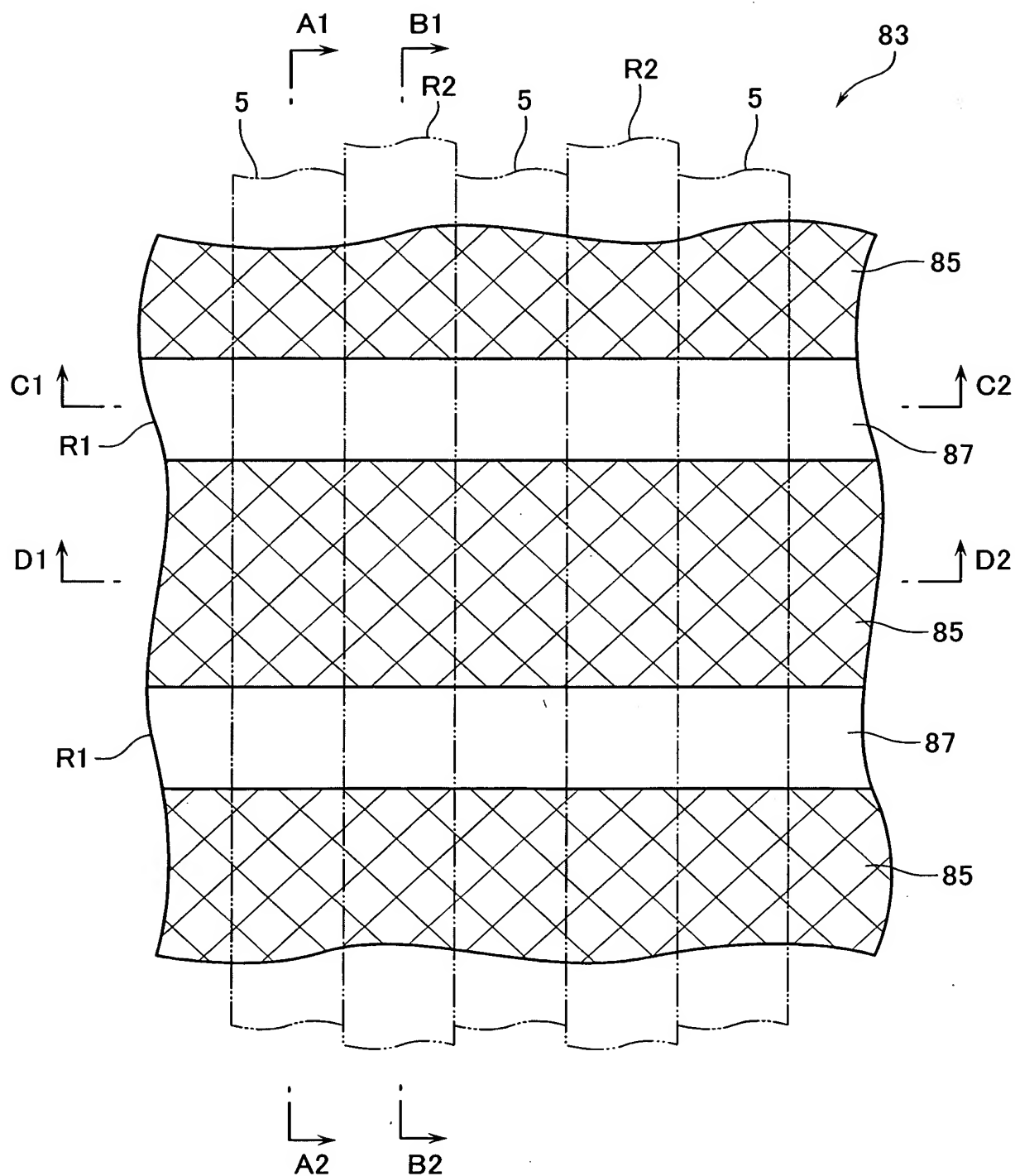




FIG. 30

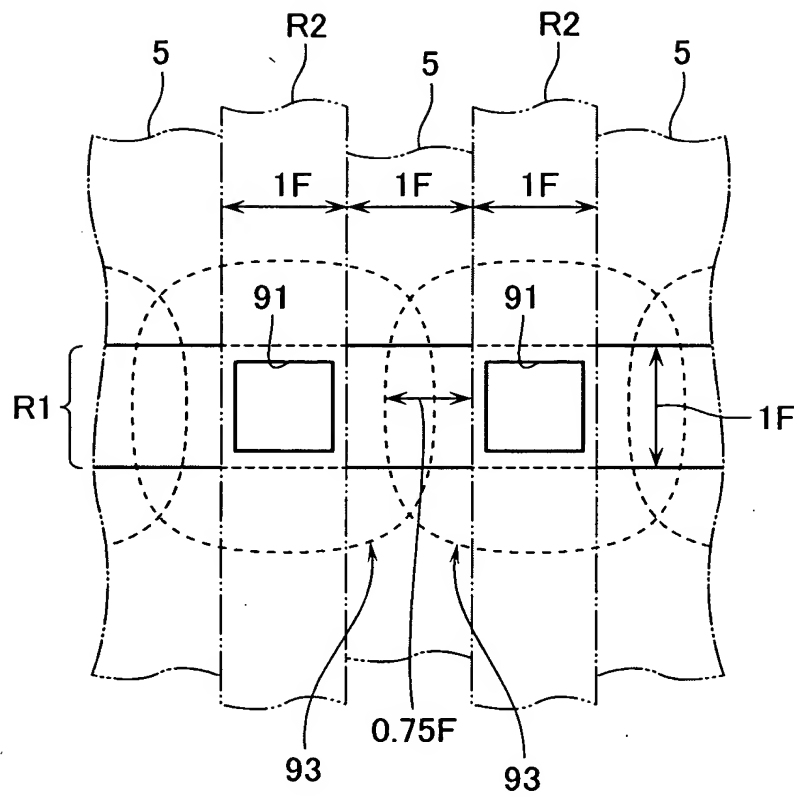


FIG. 31

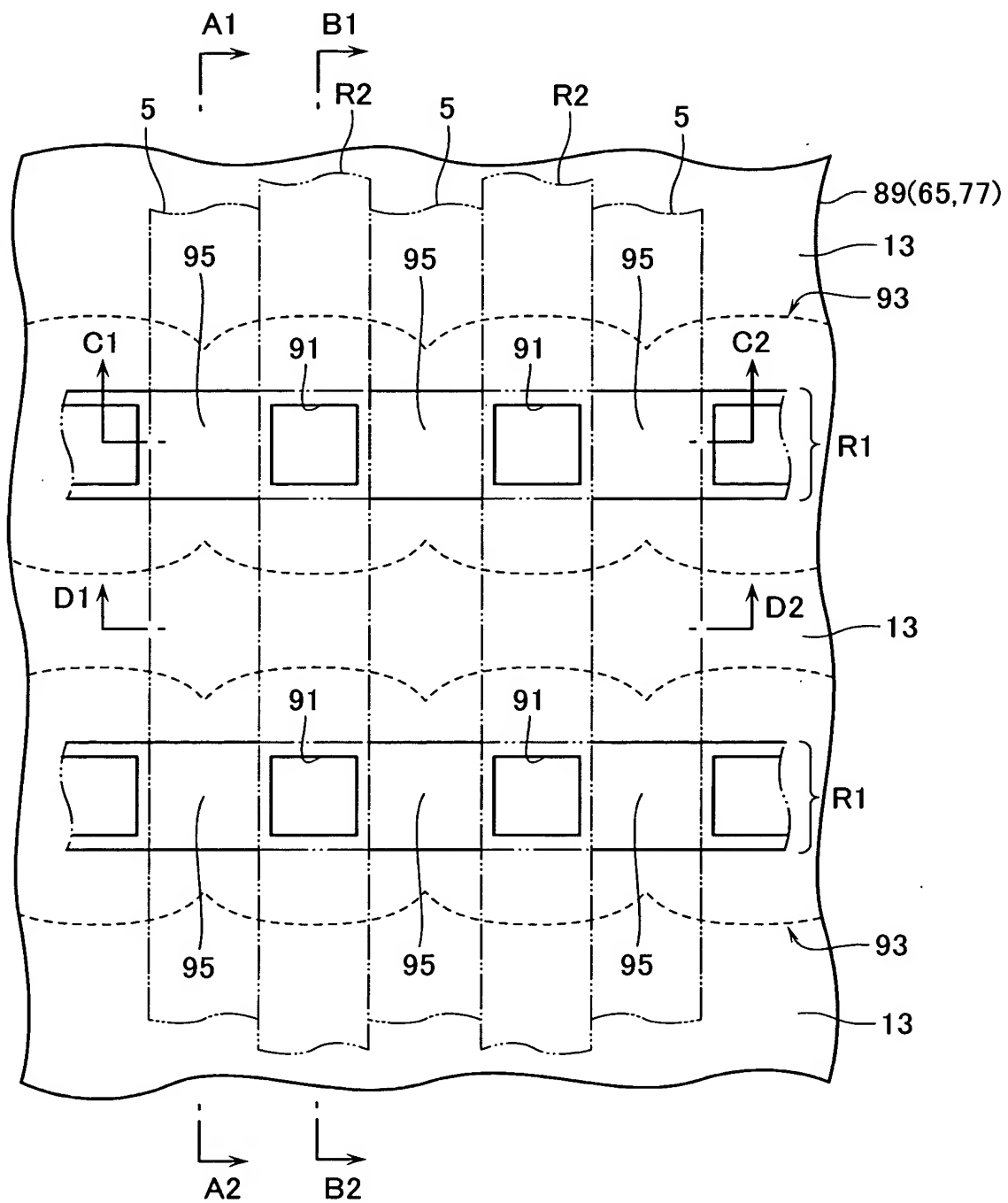


FIG. 32

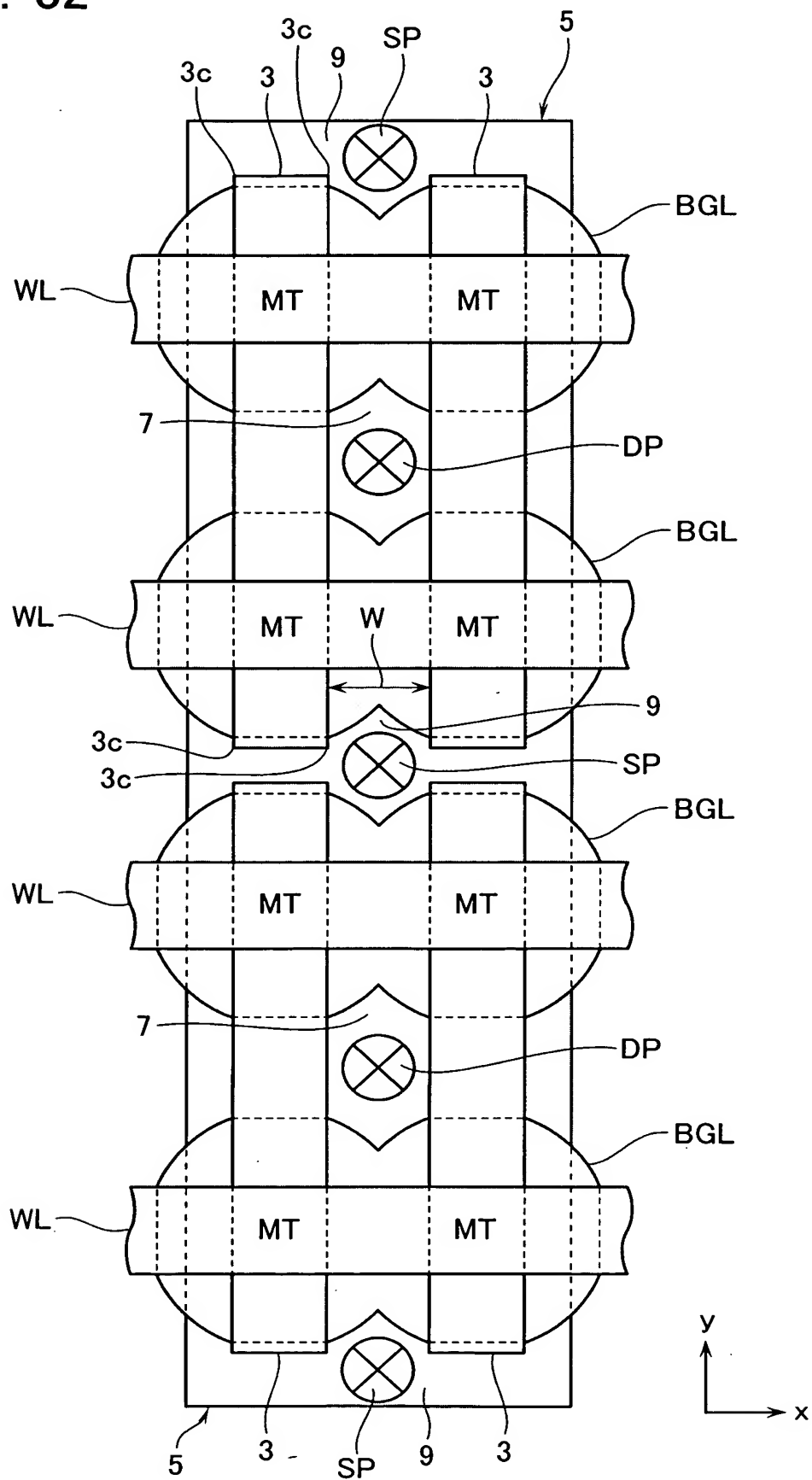
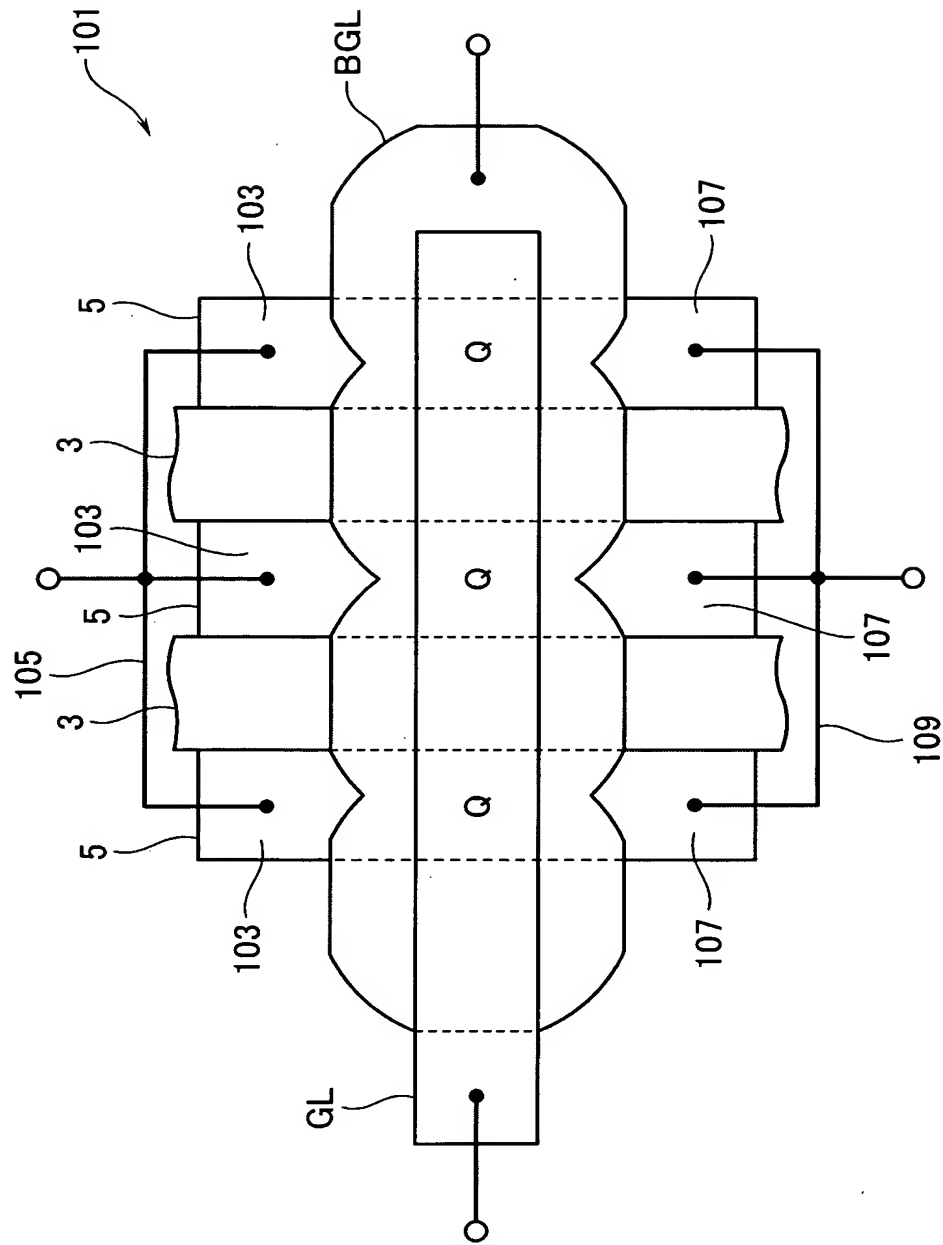




FIG. 33



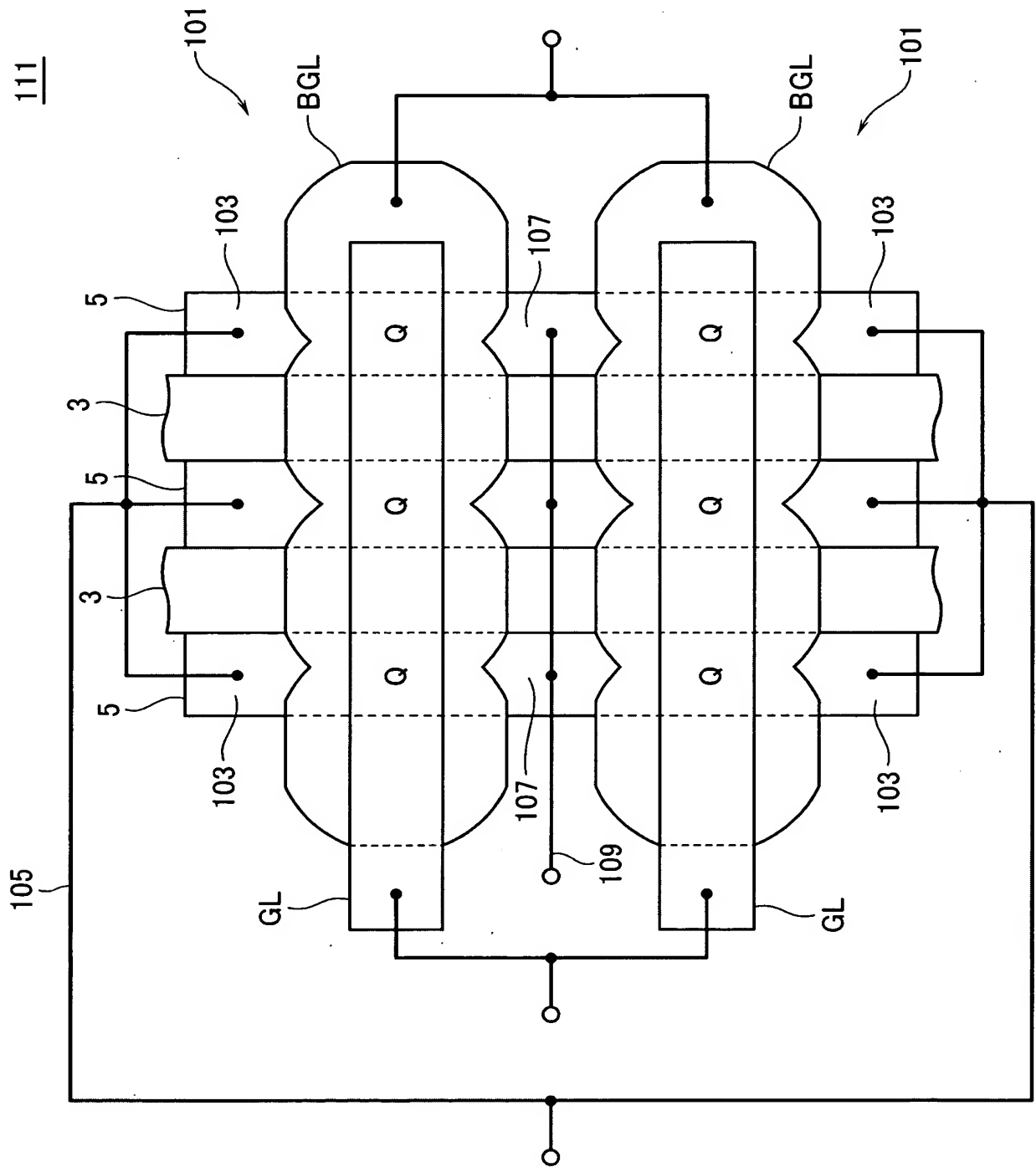


FIG. 34